JW5121

60V/2A Asynchronous Step-Down Converter

DESCRIPTION

The JW®5121 is a current mode monolithic buck switching regulator. Operating with an input range of 4.5V~60V, the JW5121 delivers 2A of continuous output current with an integrated high side N-Channel MOSFET. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripple. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The JW5121 guarantees robustness with short-circuit protection, thermal protection, current run-away protection, and input under voltage lockout.

The JW5121 is available in 8-pin ESOP and 10-pin EMSOP package, which provides a compact solution with minimal external components.

FEATURES

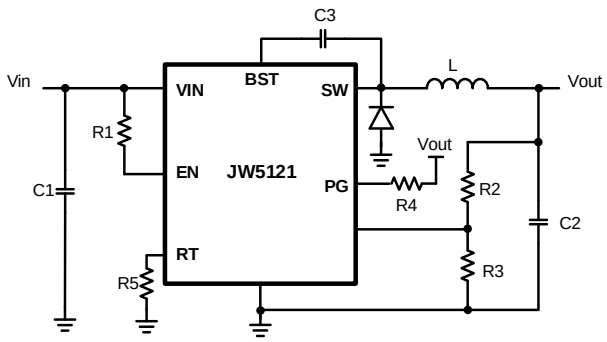
- 4.5V to 60V operating input range
  2A output current
- High efficiency at light load
- Internal soft-start
- Adjustable switching frequency
- Input under voltage lockout
- Current run-away protection
- Short circuit protection
- Thermal protection
- Available in ESOP8 and EMSOP10 package

APPLICATIONS

- Distributed Power Systems
- Automotive Systems
- High Voltage Power Conversion
- Industrial Power Systems
- Battery Powered Systems

TYPICAL APPLICATION

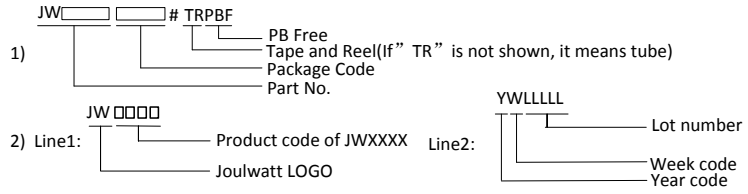
Step Down Regulators



ORDER INFORMATION

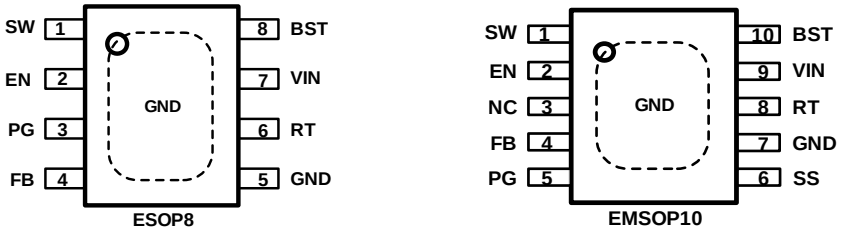
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5121ESOP#TRPBF	ESOP8	JW5121 YWLLLLL
JW5121EMSOP#TRPBF	EMSOP10	JW5121 YWLLLLL

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, SW Pin ..... -0.3V to 66V
BST Pin ..... SW-0.3V to SW+5V
PG Pin ..... -0.3V to 22V
All other Pins ..... -0.3V to 6V
Junction Temperature[2) 3)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN .....4.5V to 60V
Output Voltage Vout.....0.8V to Dmax x VIN V
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
ESOP8	50...	10ºC/W
EMSOP10.....	60...	30ºC/W

Note：

1) Exceeding these ratings may damage the device.

2) The JW5121 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW5121 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
V_{IN} Under Voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising		3.6		V
V_{IN} Under Voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			200		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		1	4	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1V		130	160	μA
Feedback Voltage	V_{FB}	4.5V<V_{VIN}<60V	788	800	812	mV
Power Switch Resistance	$R_{DS(ON)T}$			285		mΩ
Power Switch Leakage Current	I_{LEAK}	V_{IN}=60V, V_{EN}=0V, V_{SW}=0V			1	uA
Power Switch Current Limit	I_{LIM}	Minimum Duty Cycle	3.2	3.5	3.8	A
Switch Frequency	f_{SW}	R_{RT}=220k	160	200	240	kHz
Switch Frequency Range	f_{SW}		100		1400	kHz
Minimum On Time[5)]	T_{ON_MIN}			100		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0V		100		ns
Soft-start Time[5)]	T_{SS}	ESOP8		0.8		ms
Soft-start Charge Current	I_{SS}			10		uA
Power Good Lower Threshold	PG_{LTH}	FB falling		88%		V_{REF}
Power Good Upper Threshold	PG_{DTH}	FB rising		112%		V_{REF}
Power Good Sink Current	I_{PG}	V_{PG}=0.4V		2		mA
Power Good Delay	PG_{DLY}	PG from low to high		240		us
EN Shut Down Threshold Voltage	V_{EN_TH}	V_{EN} rising, FB=0.6V	1.28	1.4	1.52	V
EN Shut Down Hysteresis	V_{EN_HYST}			200		mV
Thermal Shutdown[5)]	T_{TSD}			150		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			15		°C

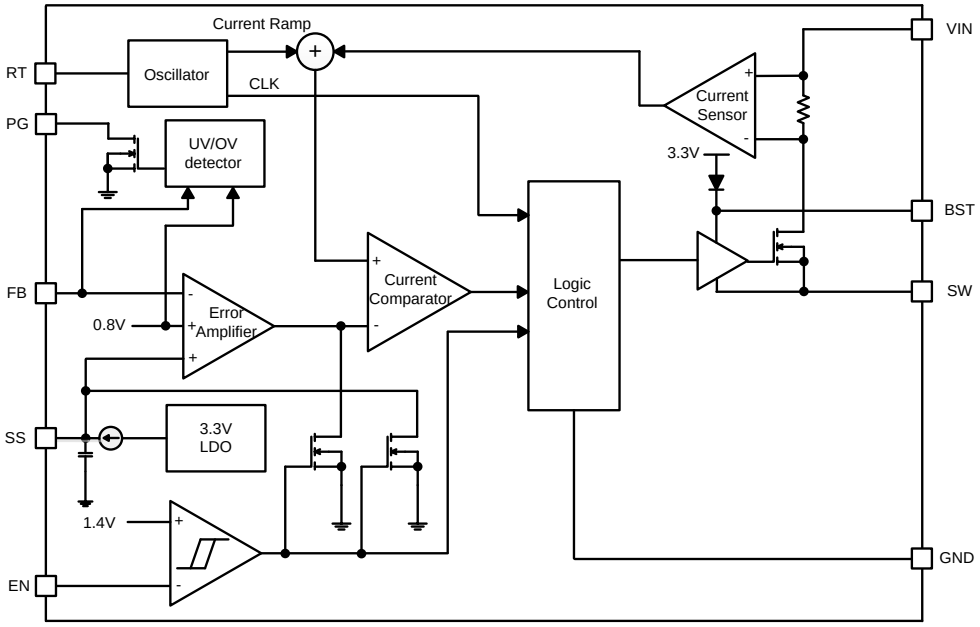
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin		Name	Description
ESOP8	EMSOP10		
1	1	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
2	2	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
3	5	PG	Open drain output for power-good flag. Use a 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 20V.
4	4	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 800mV. Connect a resistive divider at FB.
5/EP	7/EP	GND	Ground.
6	8	RT	Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency.
7	9	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 60V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
8	10	BST	Bootstrap pin for top switch.
	3	NC	
	6	SS	Soft-start control pin. Leave floating for internal soft-start slew rate. Connect to a capacitor to extend soft start time.

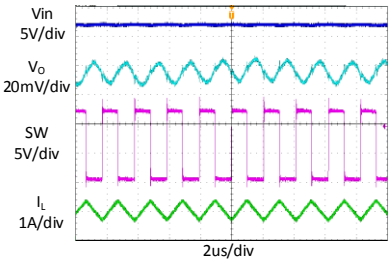
BLOCK DIAGRAM



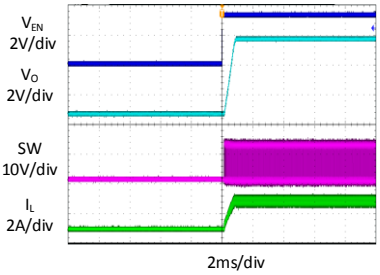
TYPICAL PERFORMANCE CHARACTERISTICS

Vin = 12V, Vout = 5V, Fs=500KHz, L = 10μH, Cout = 44μF, TA = +25°C, unless otherwise noted

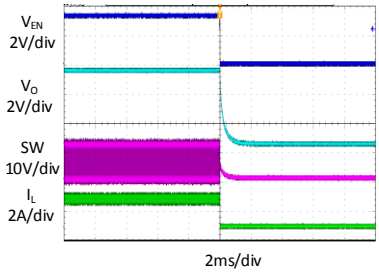
Steady State Test
Iout=2A



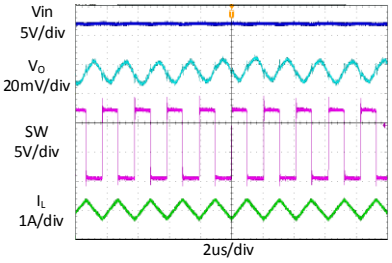
Startup through Enable
Iout=2A (Resistive load)



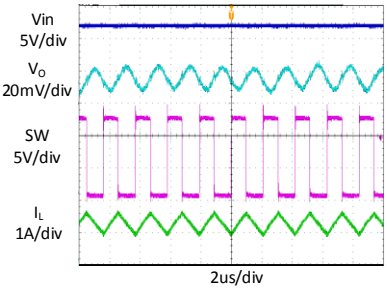
Shutdown through Enable
Iout=2A (Resistive load)



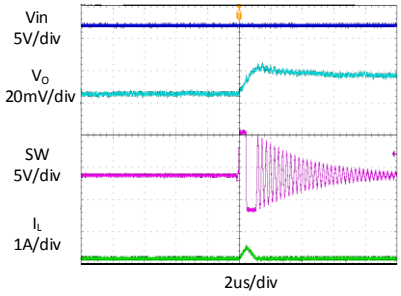
Heavy Load Operation
2A LOAD



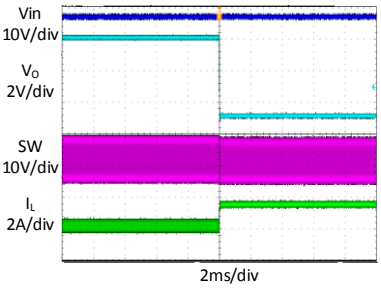
Medium Load Operation
1.1A LOAD



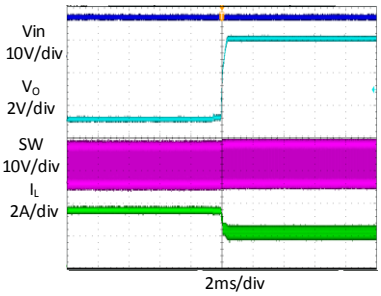
Light Load Operation
0 A LOAD



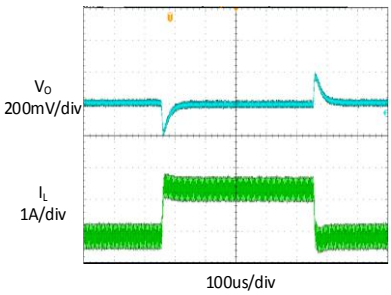
Short Circuit Protection
Iout=2A- Short



Short Circuit Protection
Iout= Short- 2A



Load Transient
0.5A LOAD → 2A LOAD →0.5A LOAD

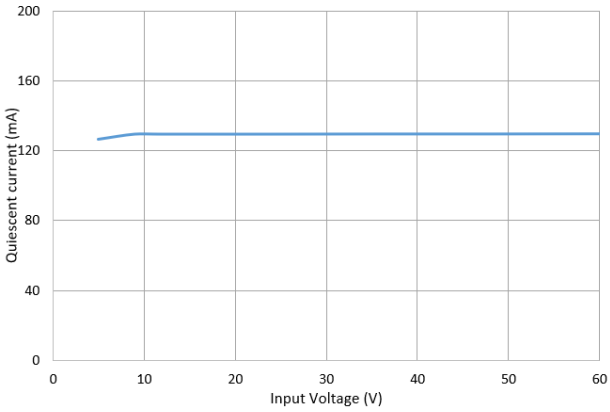


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Vout = 5V, L = 10μH, Cout = 44μF, TA = +25°C, unless otherwise noted

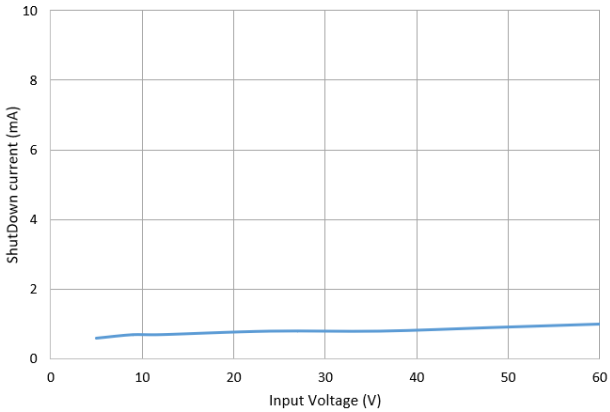
Quiescent Current Vs. Input Voltage

VIN=5V ~ 60V, VEN=3V, VFB=1V

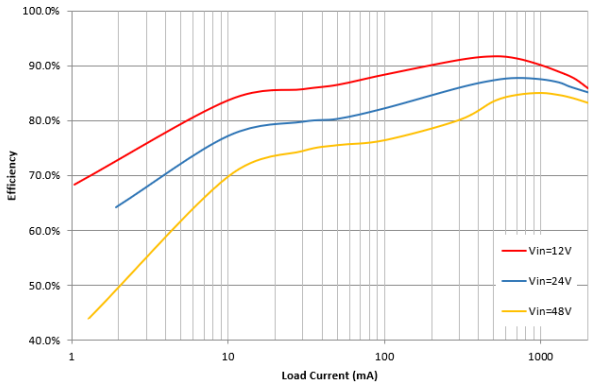


Shutdown Current Vs. Input Voltage

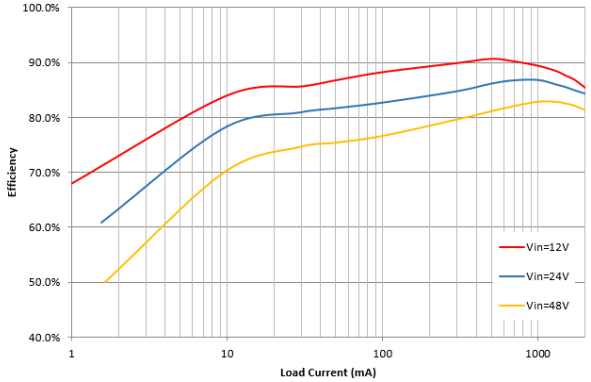
VIN=5V ~ 60V, VEN=0V, VFB=0.3V



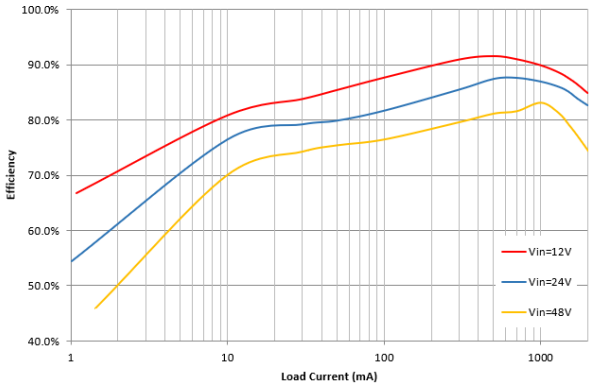
Efficiency @ 300KHz



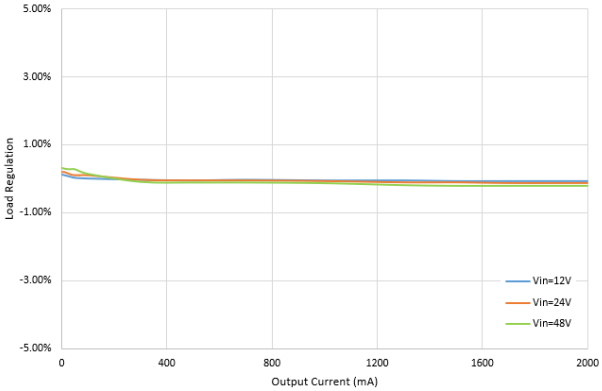
Efficiency @ 500KHz



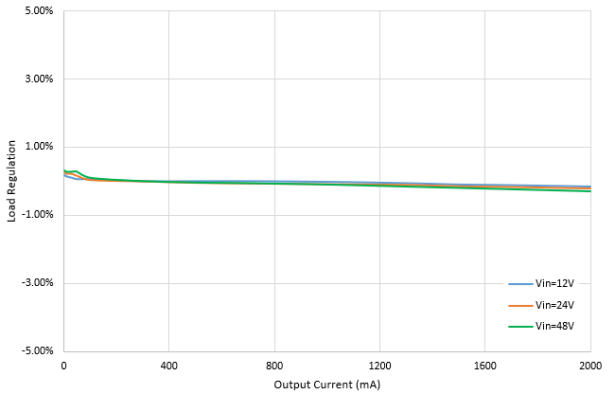
Efficiency @ 900KHz



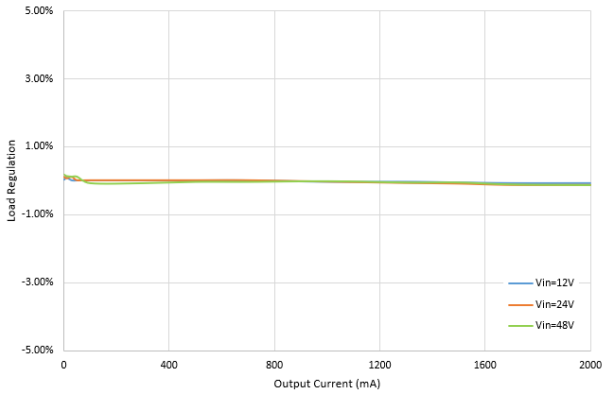
Load Regulation @ 300KHz



Load Regulation @ 500KHz



Load Regulation @ 900KHz



FUNCTIONAL DESCRIPTION

The JW5121 is an asynchronous, current-mode, step-down regulator. It regulates input voltages from 4.5V to 60V down to an output voltage as low as 0.8V, and is capable of supplying up to 2A of load current.

Current-Mode Control

The JW5121 utilizes current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier. The voltage feedback loop is compensated by an internal RC network.

Output of the error amplifier V_{COMP} is compared with the switch current measured internally to control the output current.

PFM Mode

The JW5121 operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Shut-Down Mode

The JW5121 shuts down when voltage at EN pin is below 1V. The entire regulator is off and the supply current consumed by the JW5121 drops below 1uA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5121 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.2V to trigger input under voltage lockout protection.

Internal Soft-start (ESOP8)

Soft-start is designed in JW5121 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. When the chip starts, the internal circuit generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is less than the VREF, SS overrides VREF and the error amplifier uses SS as the reference. When SS exceeds V_{REF}, VREF regains control.

Switching Frequency

The switching frequency of JW5121 can be programmed by the resistor R_T from the RT pin and GND pin over a wide range from 100 kHz to 1400 kHz. The RT pin voltage is typically 1.2V and must have a resistor to ground to set the switching frequency. The R_T resistance can be calculated by the following equation for a given switching frequency f_{SW}.

$$R_T(\Omega) = \frac{\frac{1}{f_{SW}(Hz)} - 110 * 10^{-9}}{2.31 * 10^{-11}}$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The

minimum controllable on time is typically 120 ns which limit the maximum operating frequency in applications with high input to output step down ratios.

Over Current / Output Short Protection

To protect the converter in overload conditions at higher switching frequencies and input voltages, the JW5121 implements a frequency fold-back. The oscillator frequency is divided by 2^X(X=0, 1, 2…7) if the power FET current rises above the current limit by 0.5A in a minimum detection time (typ. 60ns). The fold-back frequency depends on the number of consecutive triggers. Once the power FET is turned off by the current limit instead of minimum on time, the frequency exist fold-back state.

During short-circuit events, the inductor current may exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency fold-back effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down. With a maximum frequency fold-back ratio of 128, there is a maximum frequency at which the inductor current can be controlled by frequency fold-back protection.

Power Good

The JW5121 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as Vout) through a resistor. When the output voltage becomes within +-12% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under or higher 12%of the target value, the power good signal becomes low.

RT Short Protection

If the RT pin is detected to be short to ground, JW5121 is not allowed to switch to prevent abnormal operation state. The regulator can be reactivated again when the short condition at the RT pin is removed.

Thermal Protection

When the temperature of the JW5121 rises above 150°C, it is forced into thermal shut-down.

Only when core temperature drops below 135°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_3}{R_2 + R_3}$$

Where VFB is the feedback voltage and VOUT is the output voltage.

Choose R3 around 10kΩ, and then R2 can be calculated by:

$$R_2 = R_3 * \left(\frac{V_{OUT}}{0.8} - 1\right)$$

Too large resistance and the following table lists the recommended values.

VOUT(V)	R2(kΩ)	R3(kΩ)
5	52.5	10
12	140	10

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Where ILOAD is the load current, VOUT is the output voltage, VIN is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})$$

Where C1 is the input capacitance value, fs is the switching frequency, ΔVIN is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 4.7~10uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * (R_{ESR} + \frac{1}{8 * f_S * C_2})$$

Where C2 is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

A 22~66uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is

typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S * \Delta I_L} * (1 - \frac{V_{OUT}}{V_{IN}})$$

Where VIN is the input voltage, VOUT is the output voltage, f_s is the switching frequency, and ∆ IL is the peak-to-peak inductor ripple current.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5121 (VIN pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.

The ground plane on the PCB should be as large as possible for better heat dissipation.

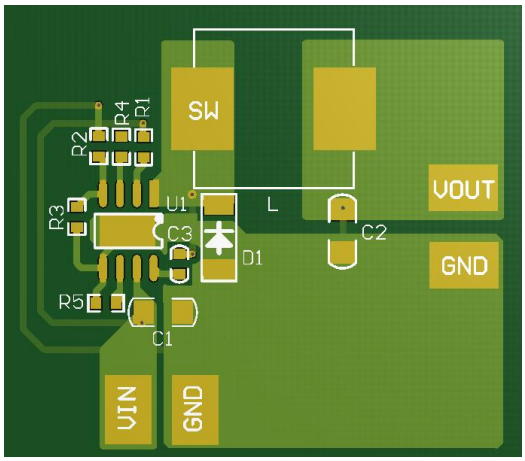


Figure1. PCB Layout Recommendation

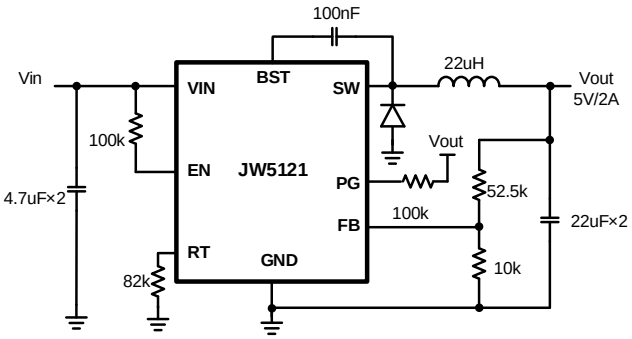
REFERENCE DESIGN

Reference 1:

Vin: 7V~60V

Vout: 5V

Iout: 0~2A

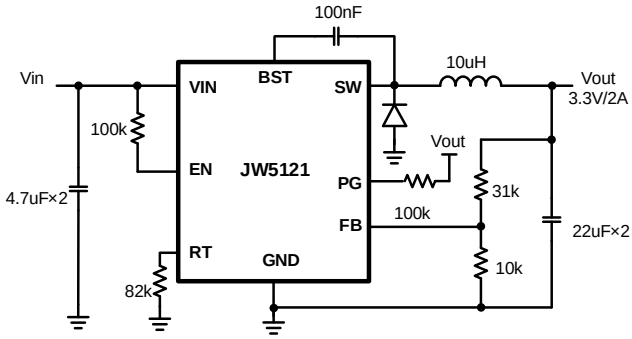


Reference 2:

Vin: 5V~60V

Vout: 3.3V

Iout: 0~2A

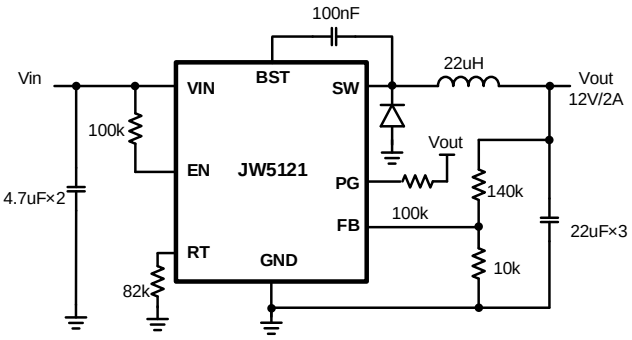


Reference 3:

Vin: 14V~60V

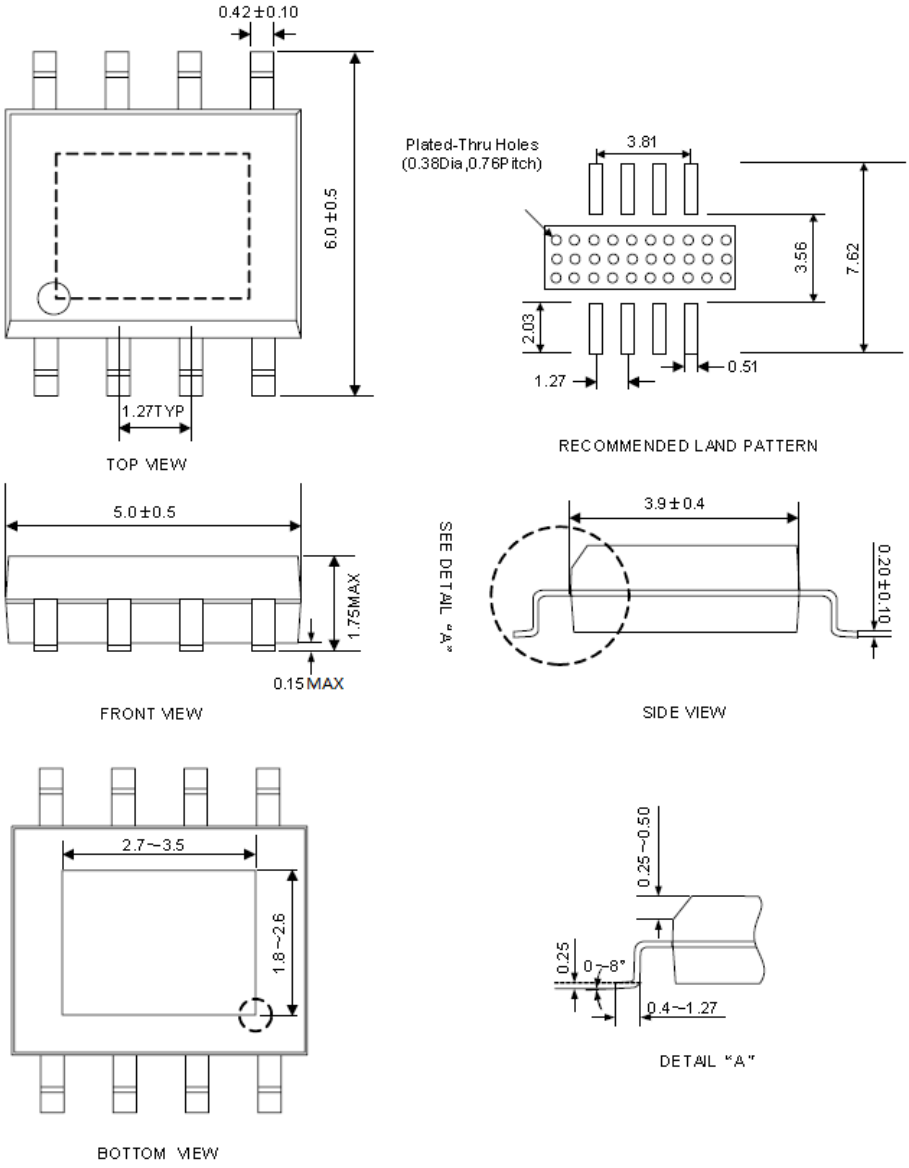
Vout: 12V

Iout: 0~2A

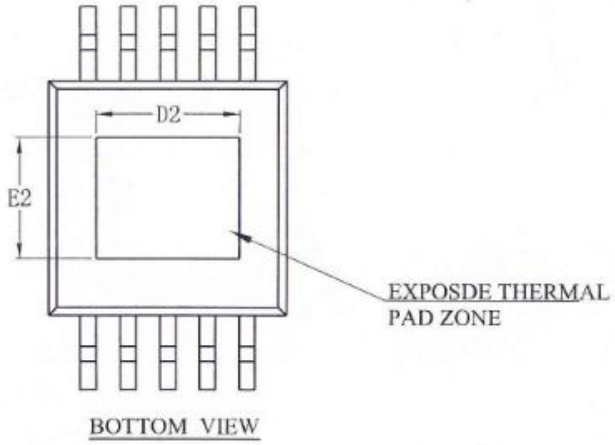


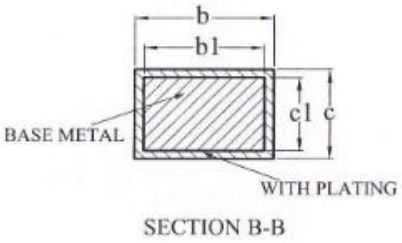
PACKAGE OUTLINE

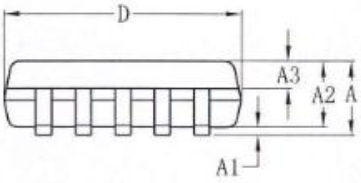
ESOP8 Unit: mm

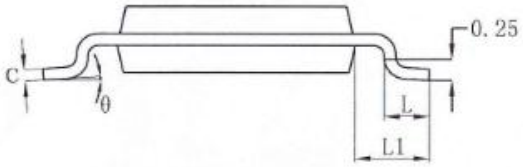


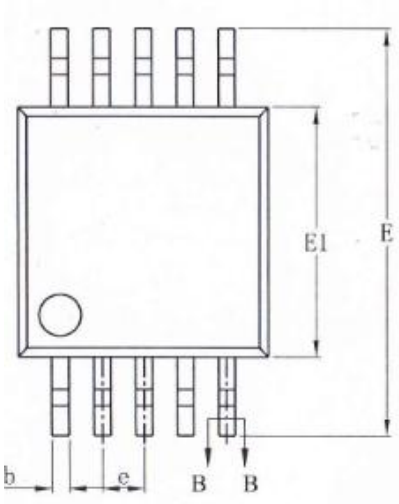
EMSOP10 UNIT: mm











SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Size(mil) / L/F Size (mil)	D2	E2
71*71	1.80REF	1.55REF