30V/6A, Peak Frequency-ADJ Synchronous Step Down Voltage Converter

1 Features

- Wide input voltage Range: 4V~30V
- Adjustable Output Voltage from 0.8 V to V_{IN}
- Low RDS(ON) Switches 22mΩ /12 mΩ
- Switching Frequency ADJ
- PFM and Forced PWM Mode Selectable
- Duty Cycle up to 100%
- Short Circuit Protection
- Over Current Protection
- Internal Soft Startup
- Thermal Shutdown Protection

2 Applications

- Car Charger
- Rechargeable Portable Devices
- Type-C Docks/Adapters
- General Purpose Point-of-Load (POL)

3 Description

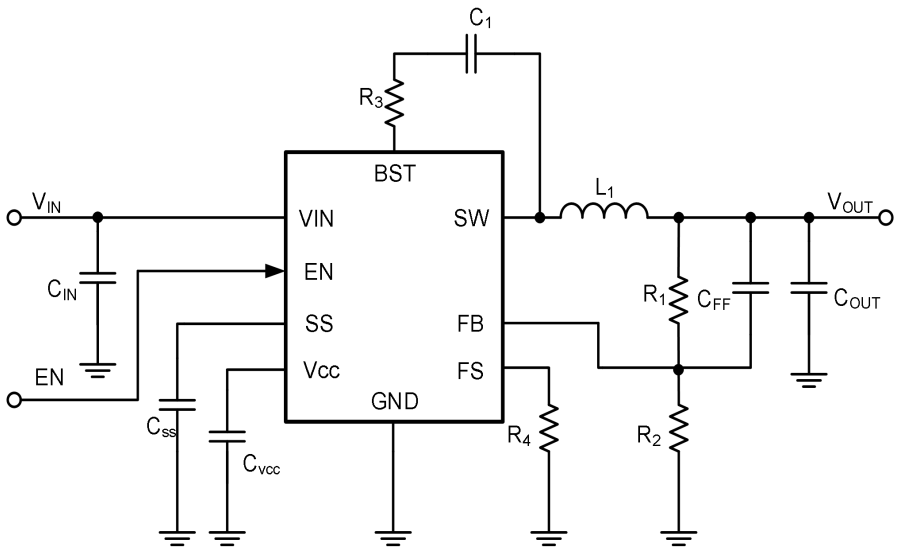
The MX8362J is a monolithic IC designed for a step-down DC/DC converter with low EMI signature, and own the ability of driving a 6A load without additional transistor. It saves board space. The MX8362J also can run at 100% duty cycle for low dropout operation, and Internal soft-start results in small inrush current extending battery life in portable systems. As a protection function, it has cycle by cycle peak current limit function, short protection function, thermal shutdown function and UVLO. The device is available in profile QFN3.5X3.5-14 package.

Device Information

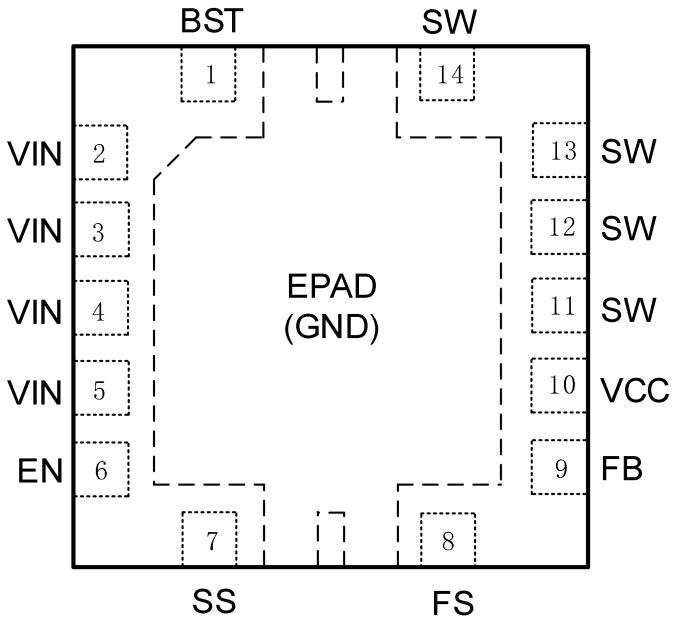
ORDERABLE DEVICE	PACKAGE TYPE	PACKAGE SIZE(mm)	DEVICE MARKING (1)
MX8362J	QFN3.5X3.5-14	3.5 x 3.5 x 0.85	MX8362J xyz

(1) "x" is year code ,"y" is Month code, "z" is lot number code.

Simplified Schematic



4 Pin Configuration and Functions



QFN3.5X3.5-14 Pin Configuration

PIN NO.	NAME	DESCRIPTION
1	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
2,3,4,5	VIN	Power supply voltage input.
6	EN	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
7	SS	Soft-Start Program Pin. Connect a capacitor (Recommend 10nF~100nF) between SS pin to GND to set the Soft-start slewrate. SS pin can't be float.
8	FS	Switching Frequency Set.Program FS to select CCM, pulse skip mode, and the operating switching frequency. Connect a resistor between FS pin and GND can configure the frequency.
9	FB	Ground pin.
10	VCC	1.0uF/6.3V capacitor connected between VCC and GND
11,12,13,14	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating temperature range(25℃) (unless otherwise noted)(1)

ITEM		MIN	MAX	UNIT
Voltage (2)	V_{IN}, EN	–0.3	33	V
	BST	–0.3	6	V
	SW (less than 10ns)(3)	–0.7	V_{IN}+0.7	V
	All Other Pins	–0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and the device is not switching. Functional operation of the device at these or any other conditions beyond those indicated under recommended perating conditions is not implied. Exposure to absolute– maximum– rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal .
(3) While switching

5.2 Recommended Operating Conditions

ITEM	MIN	MAX	UNIT
Operating junction temperature (1)	-40	125	°C/W
Operating temperature range	-40	85	°C/W
Input voltage V_{IN}	4.5	30	V
Output current	0	6.0	A

(1) All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

5.3 Electrical Characteristics

V_{IN}=12V, T_A=25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		4.0		30	V
I_Q	Quiescent current into VIN pin/CCM			15	29	mA
	Quiescent current into VIN pin/PFM			350	430	μA
I_{OFF}	Shut down current	EN = GND			3	μA
V_{FB}	Regulated Feedback Voltage		788	800	812	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
$V_{IN(UVLO)}$	V_{IN} under voltage lockout			3.3		V
	V_{IN} under voltage lockout Hysteresis			400		mV
ENABLE (EN PIN)						
$V_{(EN\_RISING)}$	Enable threshold	Rising	1.2			V
$V_{(EN\_FALLING)}$		Falling			0.8	V
$V_{(EN\_HYS)}$	Threshold Hysteresis			200		mV
POWER STAGE						
$R_{(HSD)}$	High-side FET on resistance	I_{SW}= 1000mA		22		mΩ
$R_{(LSD)}$	Low-side FET on resistance	I_{SW}=-1000mA		12		mΩ
$R_{(DISCHARGE)}$				200		Ω
VCC Regulator						

V_{CC}	VCC regulator	VIN>5.2V		5		V
I_{VCC}	VCC current limit	High to low	20			mA
CURRENT LIMIT						
$I_{(LIM\_HS)}$	High side FET current limit			7		A
$I_{(LIM\_LS)}$	Low side FET current limit			8		A
OSCILLATOR						
F_{sw}	Frequency &Mode set	FS=PGND, PFM		250		KHz
		FS=30K, PFM		300		KHz
		FS=75K, PFM		400		KHz
		FS=150K, CCM		400		KHz
		FS=270K, CCM		300		KHz
		FS= Float, CCM		250		KHz
Buck Output OVP and UVP						
$V_{(OVP\_rising\_th)}$	Output OVP rising threshold			115%		V_{FB}
$V_{(OVP\_falling\_th)}$	Output OVP falling threshold			105%		V_{FB}
$V_{(UVP\_falling\_th)}$	UVP falling threshold			75%		V_{FB}
$V_{(UVP\_rising\_th)}$	UVP rising threshold			85%		V_{FB}
OVER TEMPERATURE PROTECTION						
Thermal Shutdown	Rising temperature			160		°C
	Hysteresis			30		°C
T_{SS}	Soft-start time		3	6	10	ms
I_{SS}	Soft-start current			10		μA
T_{ON_MIN}	Minimum switch on time			70		ns
T_{OFF_MIN}	Minimum switch off time			150		ns

6 Detailed Description

6.1 Overview

The MX8362J DC/DC converter is designed to provide up to a 6A output from an input voltage source of 4V to 30V. The MX8362J is a high output current monolithic switch-mode step-down DC-DC converter. The internal compensation makes feedback control having good line and load regulation without external design.Regarding protected function, thermal shutdown is to prevent over temperature operating from damage, and current limit is against over current operating of the output switch. If current limit function occurs and V_{FB} is down below 0.8V, the switching frequency will be reduced.

6.2 Functional Block Diagram

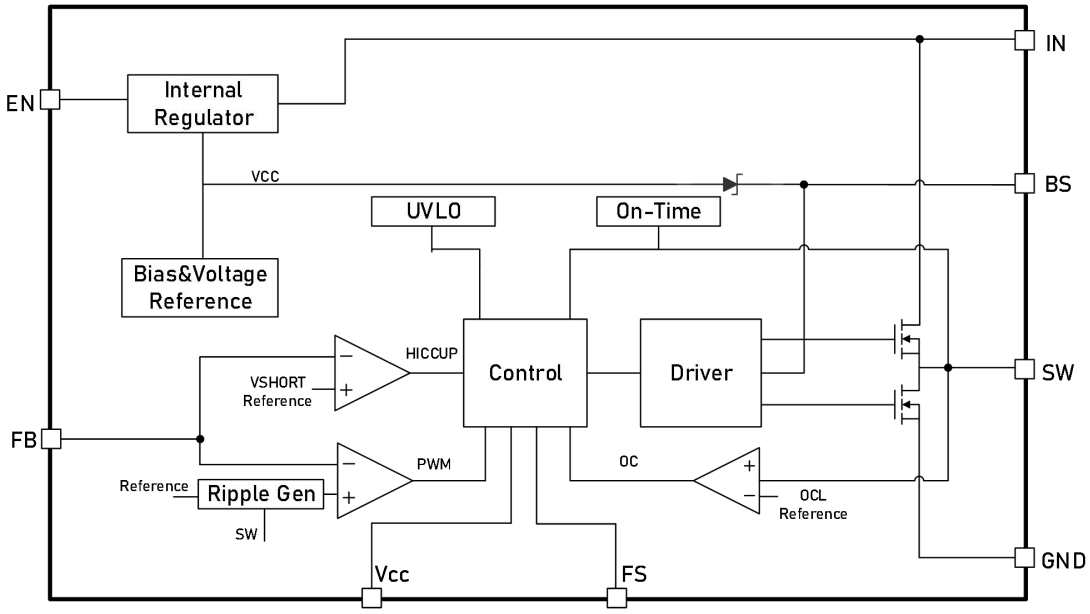
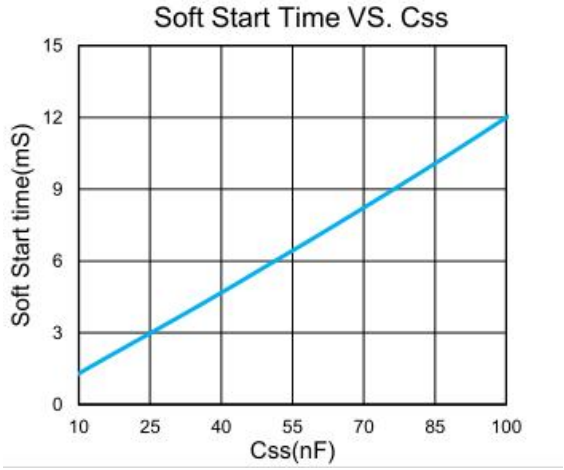


Figure 1. MX8362J Functional Block Diagram

6.3 Soft Start (SS)

The MX8362J employs an soft-start mechanism to ensure a smooth output during power-up.When the chip starts(both EN>1.25V and VIN/VCC is above UVLO), an internal current source charges up the SS capacitor. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time can be programmable by connecting a capacitor between SS pin and GND pin, the relationship of soft-start time and SS capacitor as shown below (See Figure 2),



If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

7 Application information

The MX8362J is a 4V to 30V wide input voltage range, high performance with 6A output current. The MX8362J requires few external power components (C_{IN}, C_{OUT} and L1). The output voltage can be programmed with external feedback to any voltage, ranging from 0.8V to the input voltage.

$$V_{OUT} = 0.8 \times \frac{R1 + R2}{R2}$$

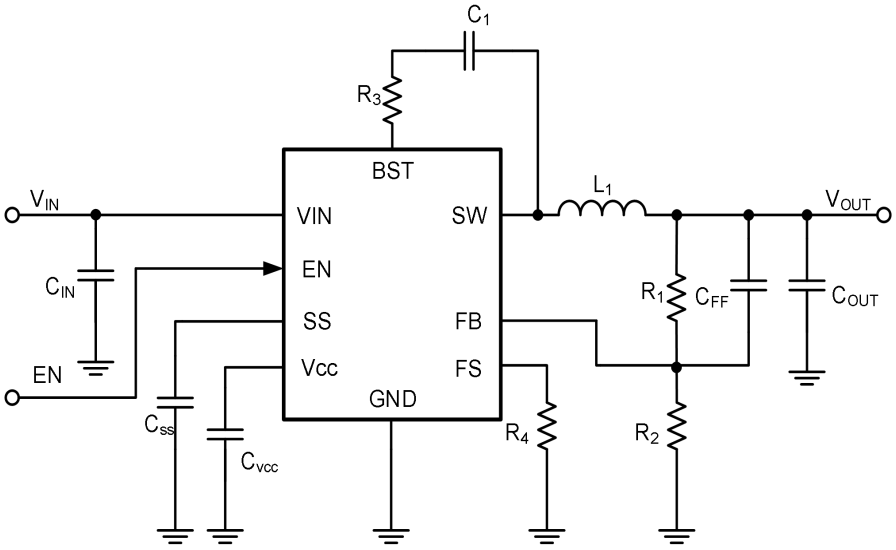


Table 7-1. Recommended Component Values

VIN(V)	V_{OUT} (V)	L1 (μH)	C1 (μF)	C_{VCC}(μF)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF} Opt.(pF)	C_{SS}(nF)	R1 (kΩ)	R2 (kΩ)
12	3.3	4.7	0.1	1	22	47+47	100	10-100	47	15
12	5	6.8	0.1	1	22	47+47	100	10-100	43	8.2
12	9	6.8	0.1	1	22	47+47	100	10-100	44	4.3
12	12	6.8	0.1	1	22	47+47	100	10-100	43	3.0
24	3.3	10	0.1	1	22	47+47	100	10-100	47	15

24	5	10	0.1	1	22	47+47	10-100	47	43	8.2
24	9	10	0.1	1	22	47+47	10-100	47	44	4.3
24	12	10	0.1	1	22	47+47	10-100	47	43	3.0
24	15	10	0.1	1	22	47+47	10-100	47	110	6.2
24	20	10	0.1	1	22	47+47	10-100	47	240	10

R3 default= 0Ω, C_{FF}: Optional C_{SS}: Optional

R4 default= NC(250KHz Mode=CCM) Frequency set :

Frequency &Mode set	FS=PGND, PFM 250 KHz	250	KHz
	FS=30K, PFM 300 KHz	300	KHz
	FS=75K, PFM 400 KHz	400	KHz
	FS=150K, CCM 400 KHz	400	KHz
	FS=270K, CCM 300 KHz	300	KHz
	FS= Float, CCM 250 KHz	250	KHz

8 Power Supply Recommendations

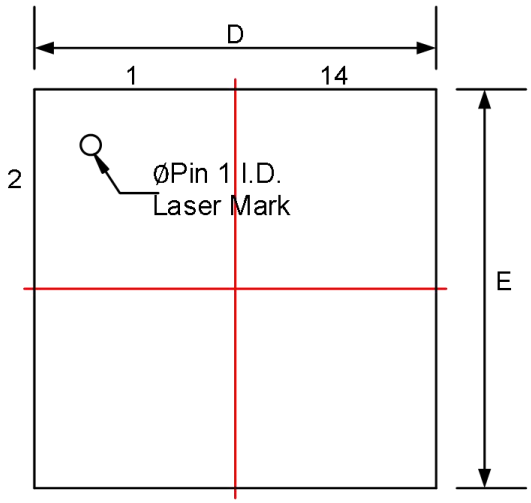
The devices are designed to operate from an input voltage supply range between 4V and 30V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μF is a typical choice.

9 Layout Guidelines

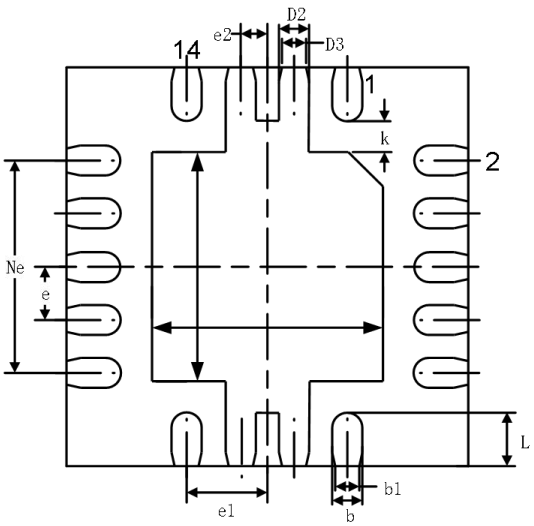
- V_{IN} and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the viewpoint of heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate V_{OUT} path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the V_{FB} node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10 Package Outline

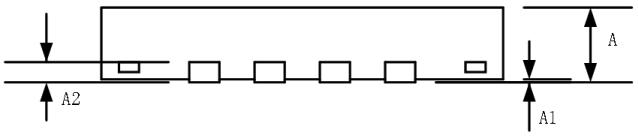
0.50QFN3.5X3.5-14-0.85



Top view



Bottom view



Front view

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	/	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
b1	0.20 REF		
D	3.40	3.50	3.60
D1	1.95	2.05	2.15
D2	0.10	0.20	0.30
D3	0.15 REF		
E	3.40	3.50	3.60
E1	1.95	2.05	2.15
E2	2.60	2.70	2.80
e	0.50 BSC		
e1	0.75 BSC		
e2	0.275 BSC		
Ne	2.00 BSC		
h	0.30 BSC		
k	0.275 REF.		
L	0.35	0.45	0.55