

*Preliminary Specifications Subject to Change without Notice*

## DESCRIPTION

The JW<sup>®</sup>5250A is a monolithic buck switching regulator based on constant on-time (COT) control for fast transient response. Operating with an input range of 2.7V-6.0V, the JW5250A delivers 1A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operate in low frequency to maintain high efficiency and low output ripples.

The JW5250A guarantees robustness with hiccup output short-circuit protection, FB short-circuit protection, start-up current run-away protection, input under voltage lockout and hot-plug in, and thermal protection.

The JW5250A is available in a 5-pin SOT23-5 package, which provides a compact solution with minimal external components.

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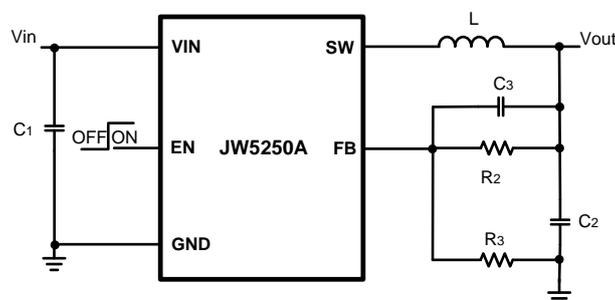
## FEATURES

- 2.7V to 6.0V operating input range
- Up to 1A output current
- Up to 92% peak efficiency
- Internal soft-start
- 1.5MHz switching frequency
- Input under voltage lockout
- Hot-plug in protection
- Short circuit protection
- Thermal protection
- Available in a SOT23-5 package

## APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- Set Top Boxes
- Telecom/Networking Systems
- Storage Equipment
- GPU/DDR Power Supply

## TYPICAL APPLICATION





**RECOMMENDED OPERATING CONDITIONS<sup>3)</sup>**

Input Voltage $V_{IN}$ .....	2.7V to 6.0V
Output Voltage $V_{out}$ .....	0.6V to $V_{IN}$
Operating Junction Temperature.....	-40°C to 125°C

**THERMAL PERFORMANCE<sup>4)</sup>**
 $\theta_{JA}$      $\theta_{JC}$ 

SOT23-5 .....	105....27°C/W
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**Note:**

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JW5250A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on a two-layer JW5250A Evaluation Board at  $T_A=25^\circ\text{C}$ .

## ELECTRICAL CHARACTERISTICS

<i>V<sub>IN</sub>=5V, T<sub>A</sub>=25°C, unless otherwise stated.</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
V <sub>IN</sub> Under Voltage Lockout Threshold	V <sub>IN_UVLO</sub>	V <sub>IN</sub> rising	2.3	2.5	2.7	V
V <sub>IN</sub> Under Voltage Lockout Hysteresis	V <sub>IN_UVLO_HYST</sub>	V <sub>IN</sub> falling		200		mV
V <sub>IN</sub> Hot-plug in Protection Threshold	V <sub>IN_OVP</sub>	V <sub>IN</sub> rising	6.1	6.6		V
V <sub>IN</sub> Hot-plug in Protection Hysteresis	V <sub>IN_OVP_HYST</sub>	V <sub>IN</sub> falling		600		mV
Shutdown Current	I <sub>SHDN</sub>	V <sub>IN</sub> =6.0V, V <sub>EN</sub> =0V		0.1	1	μA
Quiescent Current	I <sub>Q</sub>	V <sub>EN</sub> =5V, I <sub>OUT</sub> =0A, V <sub>FB</sub> =V <sub>REF</sub> *105%		40	70	μA
Regulated Feedback Voltage	V <sub>FB</sub>	2.7V<V <sub>IN</sub> <6.0V	0.588	0.6	0.612	V
PFET On Resistance <sup>5)</sup>	R <sub>DSON_P</sub>	V <sub>IN</sub> =3.6V, I <sub>SW</sub> =200mA		260		mΩ
NFET On Resistance <sup>5)</sup>	R <sub>DSON_N</sub>	V <sub>IN</sub> =3.6V, I <sub>SW</sub> =-200mA		190		mΩ
PFET Leakage Current	I <sub>LEAK_P</sub>	V <sub>IN</sub> =6.0V, V <sub>EN</sub> =0V, V <sub>SW</sub> =0V			1	uA
NFET Leakage Current	I <sub>LEAK_N</sub>	V <sub>IN</sub> =6.0V, V <sub>EN</sub> =0V, V <sub>SW</sub> =6.0V			1	uA
PFET Current Limit <sup>5)</sup>	I <sub>LIM_TOP</sub>		1.6	2.0	2.4	A
NFET Current Limit <sup>5)</sup>	I <sub>LIM_BOT</sub>		1.2	1.5	1.8	A
Switch Frequency	F <sub>SW</sub>	I <sub>OUT</sub> =1A		1.5		MHz
Minimum On Time <sup>5)</sup>	T <sub>ON_MIN</sub>			100		ns
Maximum Duty Cycle <sup>5)</sup>	D <sub>MAX</sub>			100		%
EN Input Logic High Voltage	V <sub>EN_H</sub>	V <sub>EN</sub> rising, FB=0.3V	1.5			V
EN Input Logic Low Voltage	V <sub>EN_L</sub>	V <sub>EN</sub> falling, FB=0.3V			0.4	V
Thermal Shutdown Threshold <sup>5)</sup>	T <sub>SHDN</sub>			150		°C
Thermal Shutdown Hysteresis	T <sub>HYST</sub>			20		°C

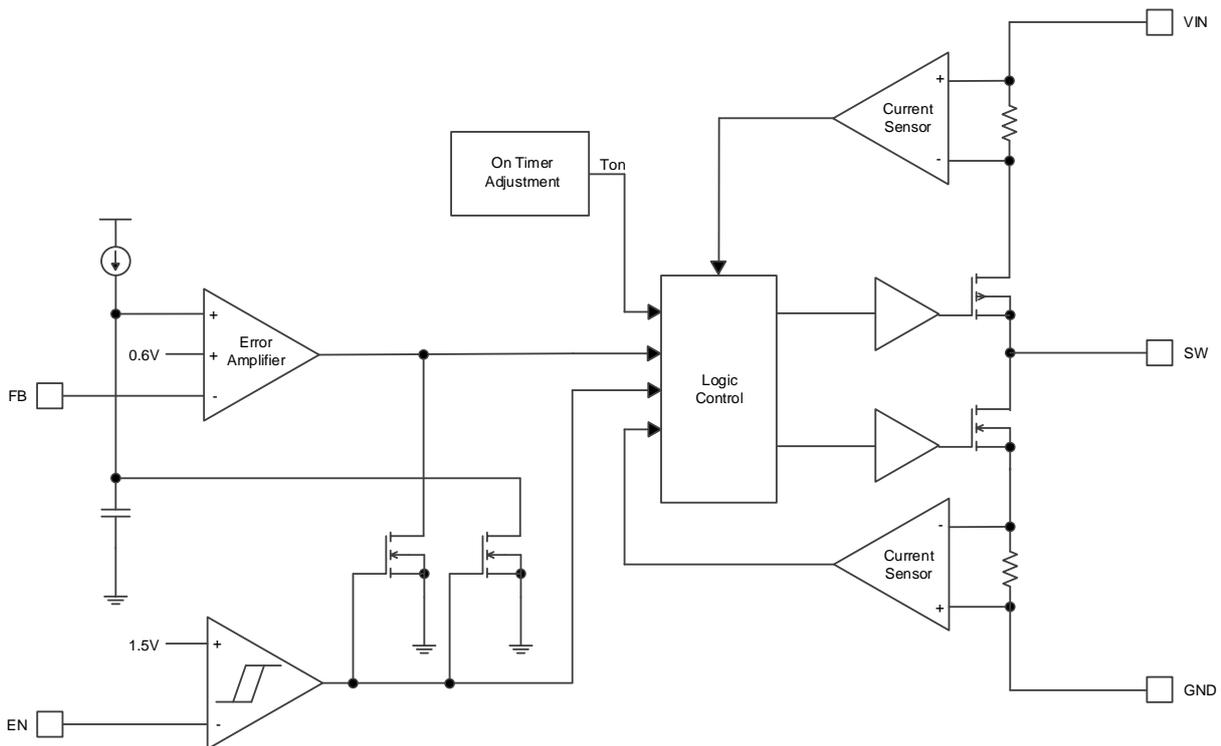
**Note:**

5) Guaranteed by design

## PIN DESCRIPTION

Pin		Name	Description
SOT23-5	SOT563		
1	5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
2	2	GND	Ground pin.
3	4	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
4	3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 2.7V to 6.0V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
5	1	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
	6	NC	

## BLOCK DIAGRAM

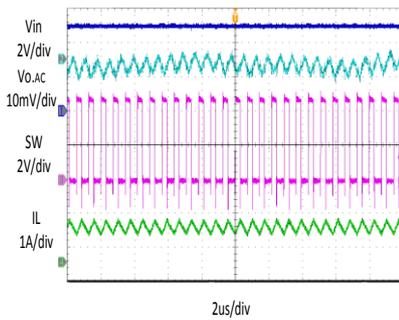


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{in} = 5V$ ,  $V_{out} = 1.8V$ ,  $L = 1.5\mu H$ ,  $C_{out} = 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted

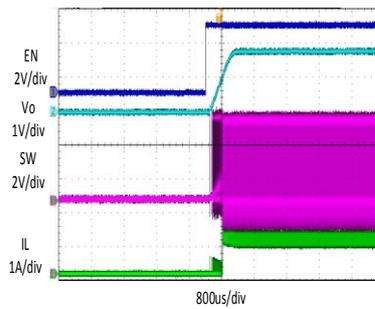
### Steady State Test

$V_{in}=5V$ ,  $V_{out}=1.8V$   
 $I_{out}=1A$



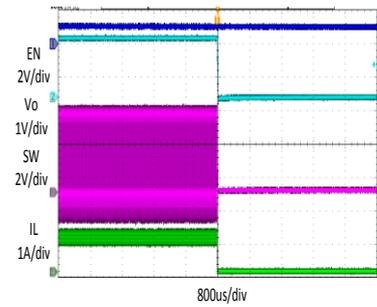
### Startup through Enable

$V_{in}=5V$ ,  $V_{out}=1.8V$   
 $I_{out}=1A$  (Resistive load)



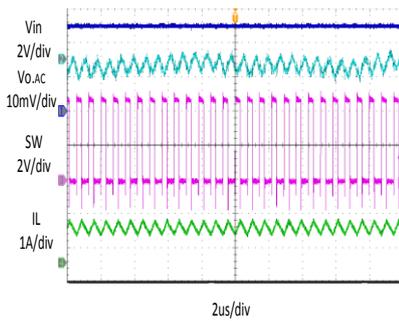
### Shutdown through Enable

$V_{in}=5V$ ,  $V_{out}=1.8V$   
 $I_{out}=1A$  (Resistive load)



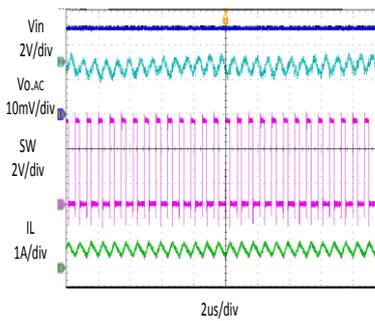
### Heavy Load Operation

1A LOAD



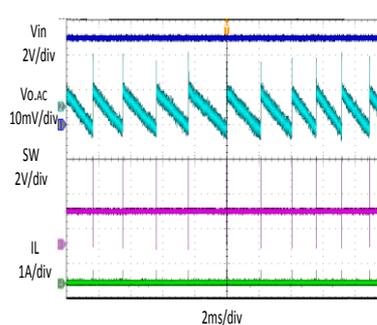
### Medium Load Operation

0.5A LOAD



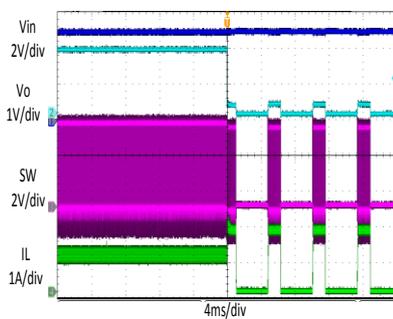
### Light Load Operation

0 A LOAD



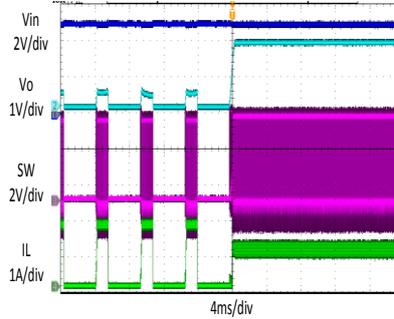
### Short Circuit Protection

$V_{in}=5V$ ,  $V_{out}=1.8V$   
 $I_{out}=1.0A$  - Short



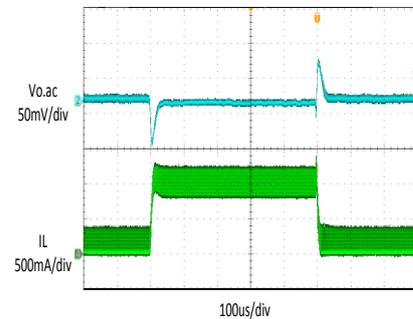
### Short Circuit Protection

$V_{in}=5V$ ,  $V_{out}=1.8V$   
 $I_{out}$  = Short-1.0A



### Load Transient

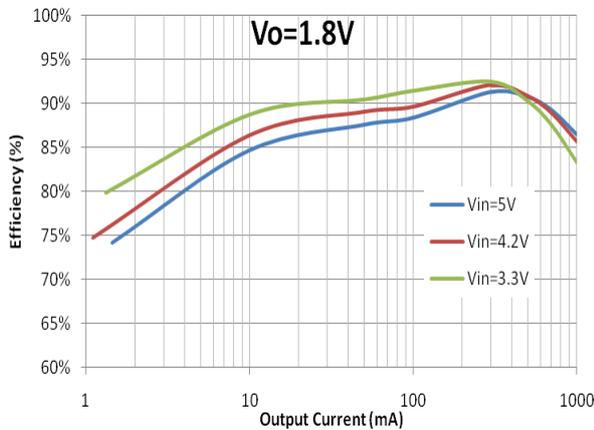
LOAD: 0.1A  $\rightarrow$  1.0A  $\rightarrow$  0.1A  
2.5A/ $\mu s$ ,  $C_{ff}=1nF$



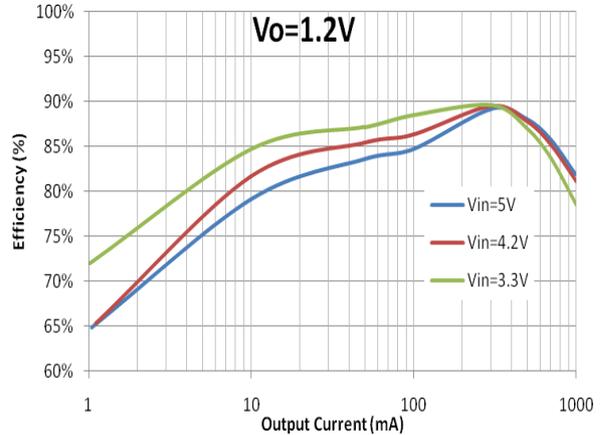
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{in} = 5V$ ,  $V_{out} = 1.8V$ ,  $L = 1.5\mu H$ ,  $C_{out} = 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted

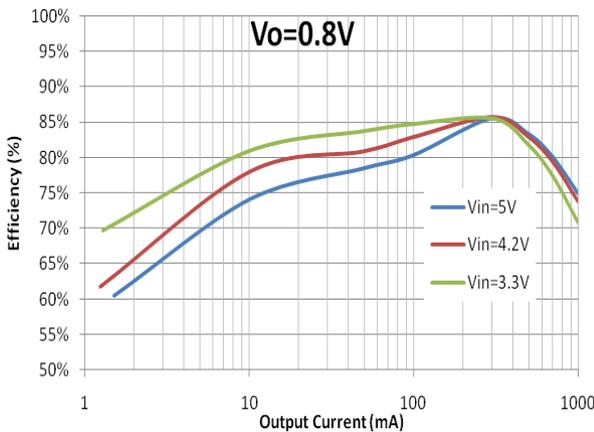
Efficiency @  $V_{out}=1.8V$



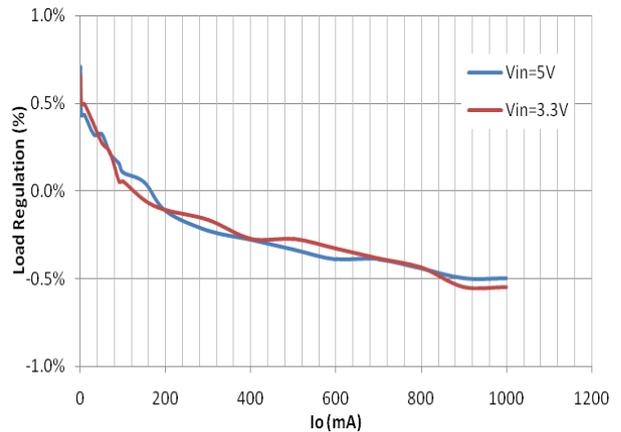
Efficiency @  $V_{out}=1.2V$



Efficiency @  $V_{out}=0.8V$

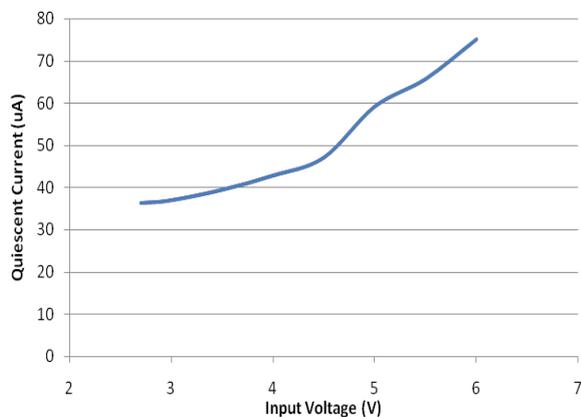


Load regulation @  $V_{out}=1.8V$



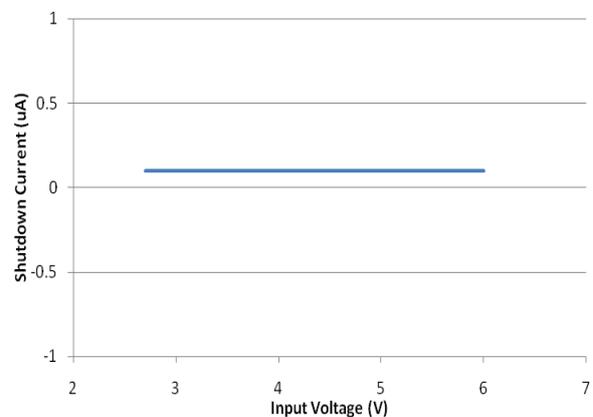
Quiescent Current Vs. Input Voltage

$V_{IN}=2.7V \sim 6V$ ,  $V_{EN}=2.5V$ ,  $V_{FB}=0.8V$



Shutdown Current Vs. Input Voltage

$V_{IN}=2.7V \sim 6V$ ,  $V_{EN}=0V$ ,  $V_{FB}=0.5V$



## FUNCTIONAL DESCRIPTION

The JW5250A is a constant on-time control, synchronous, step-down regulator. It regulates input voltages from 2.7V~6.0V down to an output voltage as low as 0.6V, and is capable of supplying up to 1A of load current.

### Constant On-time Control

The JW5250A utilizes constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.

Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

### PFM Mode

The JW5250A operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

### Shut-Down Mode

The JW5250A operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JW5250A drops below 1 $\mu$ A.

### Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5250A to down convert the input voltage to the regulated output voltage.

### Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 8ms. This procedure is repeated as long as short circuit condition is not removed.

### FB Short Circuit Protection

When FB is shorted to ground and holds for more 16 cycles, NFET will be turned off after inductor current drops to zero, and then both PFET and NFET are latched off. When short circuit condition is removed, it can be recovery.

### Hot Plug-in Protection

When input voltage is greater than hot plug-in protection threshold, typical 6.8V, it will disable JW5250A. When input voltage decrease below 6.4V, it will be enabled again.

### Thermal Protection

When the temperature of the JW5250A rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator becomes active again.

## APPLICATION INFORMATION

### Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_3}{R_2 + R_3}$$

where  $V_{FB}$  is the feedback voltage and  $V_{OUT}$  is the output voltage.

Choose  $R_3$  around 10K $\Omega$ , and then  $R_2$  can be calculated by:

$$R_2 = R_3 \cdot \left( \frac{V_{OUT}}{0.6V} - 1 \right)$$

The following table lists the recommended values.

Vout(V)	R2(K $\Omega$ )	R3(K $\Omega$ )
1.2	10	10
1.8	20	10
2.5	31.6	10
3.3	49.9	11

### Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where  $I_{LOAD}$  is the load current,  $V_{OUT}$  is the output voltage,  $V_{IN}$  is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where  $C_1$  is the input capacitance value,  $f_s$  is the switching frequency,  $\Delta V_{IN}$  is the input ripple current.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1 $\mu$ F, should be placed closer than 3mm to the IC as possible when using electrolytic capacitors.

A 10 $\mu$ F/0805/10V~22 $\mu$ F/0805/10V ceramic capacitor is recommended in typical application.

### Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left( R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2} \right)$$

where  $C_2$  is the output capacitance value and  $R_{ESR}$  is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22 $\mu$ F/0805/6.3V~44 $\mu$ F/0805/6.3V ceramic capacitor is recommended in typical application.

### Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the

output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $f_s$  is the switching frequency, and  $\Delta I_L$  is the peak-to-peak inductor ripple current.

### PCB Layout Note

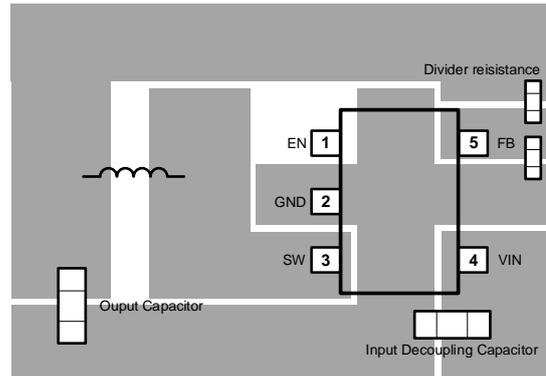
The following advice should be considered when laying out a printed circuit board for the JW5250A.

1. Place the input decoupling capacitor as close to JW5250A (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized. IC cannot work

well when  $V_{in}$  pin is interfered by noise.

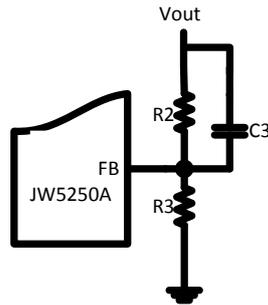
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

### Layout Example



## External Components Suggestion:

V <sub>OUT</sub> (V)	R <sub>2</sub> (kΩ)	R <sub>3</sub> (kΩ)	C <sub>3</sub> (nF)	L(μH)	C <sub>out</sub> (μF)
1	6.8	10.2	NC~1	1~2.2	20~44
1.2	10	10	NC~1	1~2.2	20~44
1.8	20	10	NC~1	1~2.2	20~44
3.3	49.9	11	NC~1	1~2.2	20~44



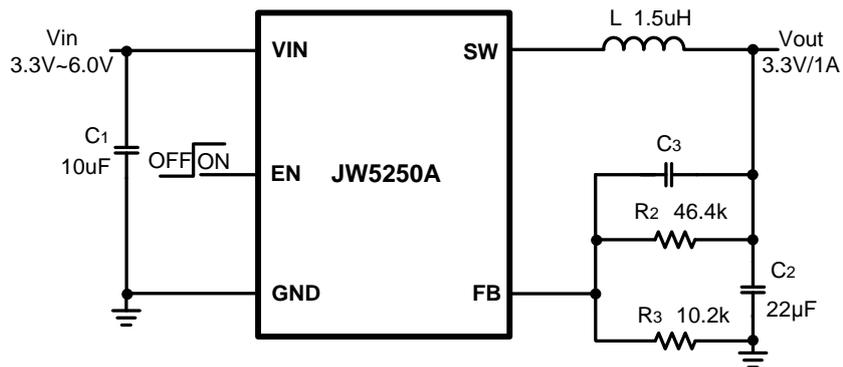
## REFERENCE DESIGN

### Reference 1:

$V_{IN}$  : 3.3V ~ 6.0 V

$V_{OUT}$ : 3.3V

$I_{OUT}$  : 0~1A

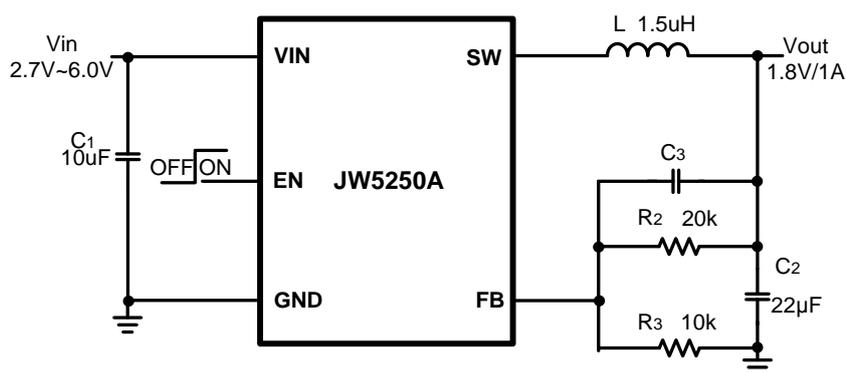


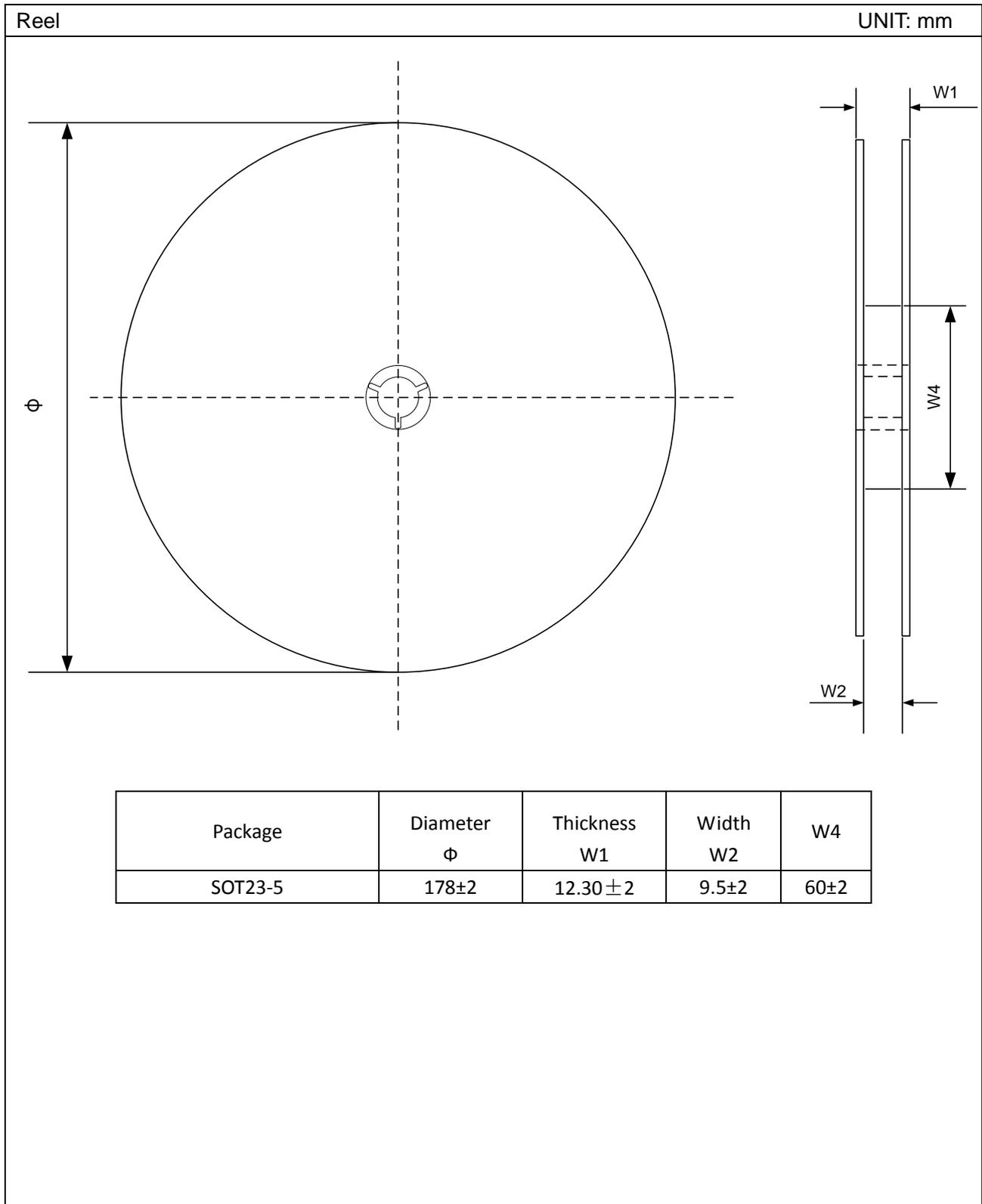
### Reference 2:

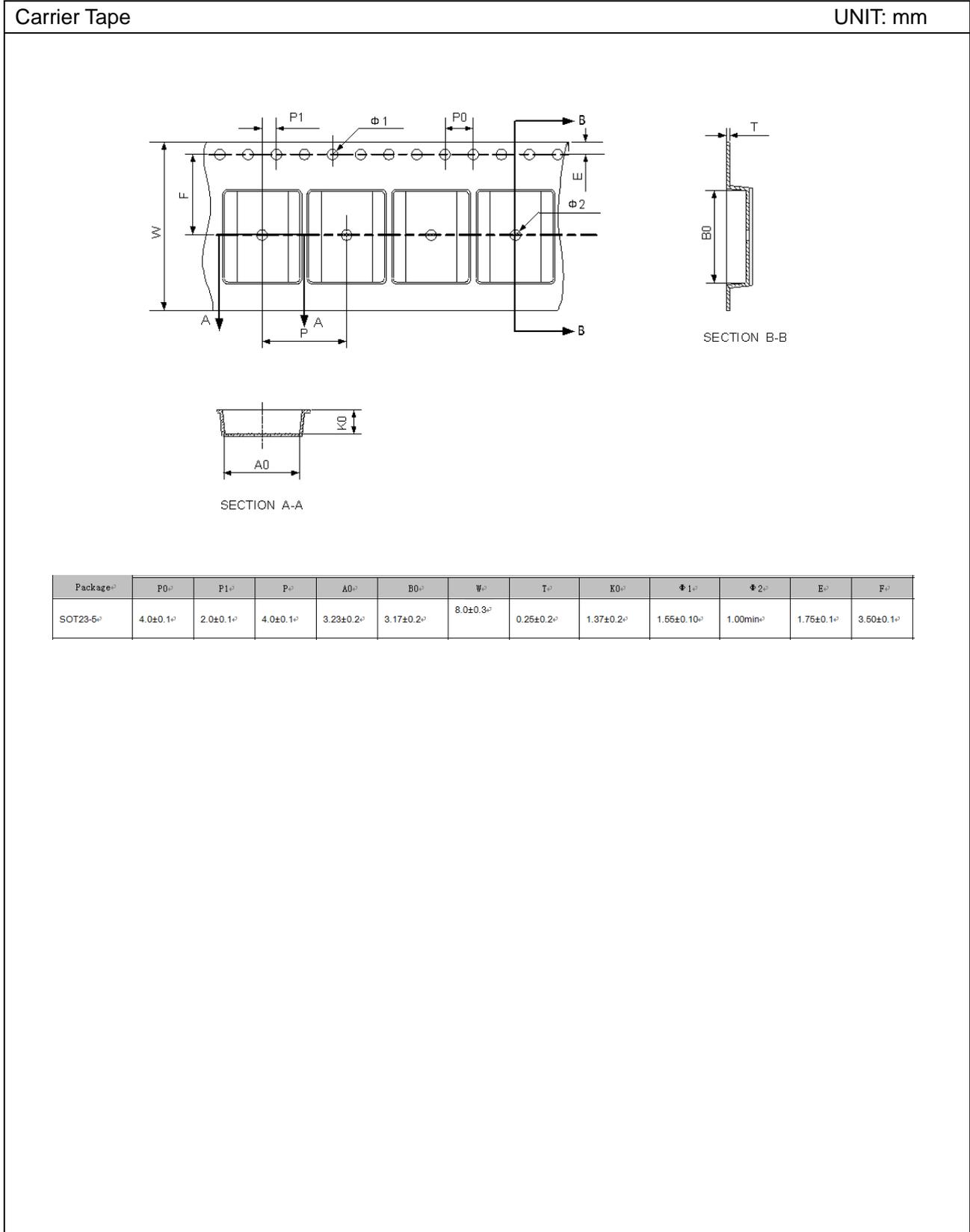
$V_{IN}$  : 2.7V ~ 6.0 V

$V_{OUT}$ : 1.8V

$I_{OUT}$  : 0~1A



**TAPE AND REEL INFORMATION**




**PACKAGE OUTLINE**

<b>SOT23-5</b>	<b>UNIT: mm</b>
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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.20	0.40	0.60
b1	0.60		
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
E2	2.40		
E3	0.80		
e	0.95 (BSC)		
e1	0.95 (TYP)		
L	0.30	0.45	0.60
θ	0°	—	8°

**Recommended Pad Layout**